LONDON SOUTH BANK UNIVERSITY

unit guide

Digital Techniques

EMI-S-714

Faculty of ESBE

2006/7

become what you want to be

Digital Techniques 2006/2007

Reference Number	EMI-S-714
Course	HND, HNC in Electrical and Electronic Engineering
Level	S
Type	Core
Prerequisites	None
Study Hours	46 hrs lecture and laboratory and 104 hrs self study
Faculty	Faculty of ESBE
Department	ECCE
Unit Co-ordinator	Alan Howson, T407 ext 7510, howsona@lsbu.ac.uk
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Introduction

The developments that have taken place in digital electronics over the past thirty years have no parallel in any other branch of engineering. There has been an inverse relationship between cost and complexity in the hardware. Roughly the real cost of hardware has halved every year while the complexity has on average quadrupled every three years. Consider this example. In 1964 one bit of memory storage would have comprised a single JK flip-flop constructed out of discrete components and cost the equivalent of 20 hours of graduate engineers time. Today single chips contain well over one million bits of storage and have a cost equivalence of less than a tenth of a second of an engineer's time per bit.

Aims

1. Clear understanding of the distinction between analogue and digital quantities.
2. Appreciate the need for different types of coding.
3. Analyse and design combinational logic circuits.
4. Analyse sequential logic circuits.
5. Understand the modular nature of digital circuits.

Core Reading

Digital Electronics (7th Ed.) Roger William Kleitz,
Prentice Hall ISBN 0-13-114165-1.

Teaching program

Wk 1 In this section you will examine a wide range of binary codes that can be used to represent numbers. We as humans use the decimal number system, but a binary system is more suited to a machine implementation because two distinct states such as high and low voltage can readily be identified without having to make precise measurements. Methods of converting between binary and decimal will be developed.

Learning outcome To be able to:

1) Distinguish between analogue and digital quantities
2) Understand the binary number system.
3) Specify the essential properties of a weighed number code.
4) Understand the difference between BCD, Gray code and straight binary codes.

Wk 2 Logic operations can be divided into 3 broad inter-related groups. In a combinational operation, the output at a given time is a function of the inputs at that instant. In a sequential operation, the output is a function of a series of inputs over a given period of time. A storage operation can hold input data and output it at a later time.

Learning outcome To be able to

1) To define combinational, sequential and storage operations.
2) Relate logic to propositional statements
3) To derive a truth table
4) To draw timing diagrams for a range of logic gates.

Wk 3-6 This section is concerned with the fundamental principles of combinational logic design. The standard logic forms will be defined. The SOP form has an AND level of logic immediately after the inputs followed by an OR gate and can be directly derived from the truth table. SOP form can be minimised both algebraically and more importantly using a K Map. Every gate in an SOP form circuit can be replaced by a NAND gate provided the circuit is two level throughout. The 'don't care condition will be analysed.

Learning outcome To be able to:

1) To apply Boolean algebra to logic design.
2) Analyse combinatorial logic circuits
3) Use the K map method of logic minimisation
4) Design NAND/NOR logic systems.

Wk 7 **Phase Test**

Wk 8-12 A sequential circuit is formed by applying feedback to a combinatorial logic system. Feedback creates additional internal inputs (or states) that cannot be controlled directly by external inputs. They are dependent on the previous inputs and state. A sequential circuit's behaviour is a function of all its previous inputs. The NAND and NOR latch's are basic memory devices, but have inherent timing problems. This problem is overcome with additional circuitry to produce an edge triggered device called a JK flipflop. The triggering edge comes from the clock signal. If all the circuit's fliflops are triggered simultaneously the type of sequential circuit is synchronous. Otherwise the circuit is asynchronous. The T and D flipflops will be discussed.

Learning outcome To be able to:

1) Understand the basic operation of the NAND and NOR latches
2) Understand the operation of edge triggered flipflops
3) 3) Understand the limitations of the set-reset flipflop
4) Explain the structure of the shift register
5) Draw output timing waveforms for registers and counters
6) Distinguish between synchronous and asynchronous logic
7) Understand the operation of the Schmidt trigger and the monostable multivibrator.

Assessment

Phase test	25%	(To take place in Week 7)
End of unit examination	50%	(To take place in Week 15)
Workshop	25%	

The bulk of the workshop mark will be based on your log book. Please note the below criteria will form the basis of the assessment.

Log Book criteria:

1) Clearly defined lab sessions.
2) Title and date of each experiment.
3) Objectives indicated for each experiment.
4) Clear diagrams and experimental method.
5) Clear indication of equipment and where necessary associated data sheets.
6) Observations and comments on experiment.
7) Experimental technique / aptitude.
8) Completed experiments.
9) Student attitude.

Please note that the above criteria are placed in no particular order and are not of equal importance

Workshop schedule.

There will be a 2hr. workshop session in T719 for every even week. The bulk of the work expected in these sessions will comprise an introductory set of digital experiments on the digital trainer DT 01. They will range from familiarisation of the trainer through circuits based on discrete components to MSI based circuits. The student **must** have a logbook from week 1 and keep a careful record in accordance with the criteria given in the assessment section. Please note that students are expected to attend every session and a register will be kept.